(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

10/542674

(43) International Publication Date
5 August 2004 (05.08.2004)

PCT

(10) International Publication Number
WO 2004/066478 A1

(51) International Patent Classification[7]: H02M 3/07

(21) International Application Number:
PCT/IB2003/006352

(22) International Filing Date:
24 December 2003 (24.12.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0301077.4 17 January 2003 (17.01.2003) GB
0314644.6 24 June 2003 (24.06.2003) GB

(71) Applicant *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **AYRES, John, R., A.** [GB/GB]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB). **YAMASHITA, Keitaro** [JP/JP]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

(74) Agent: **WILLIAMSON, Paul, L.**; Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

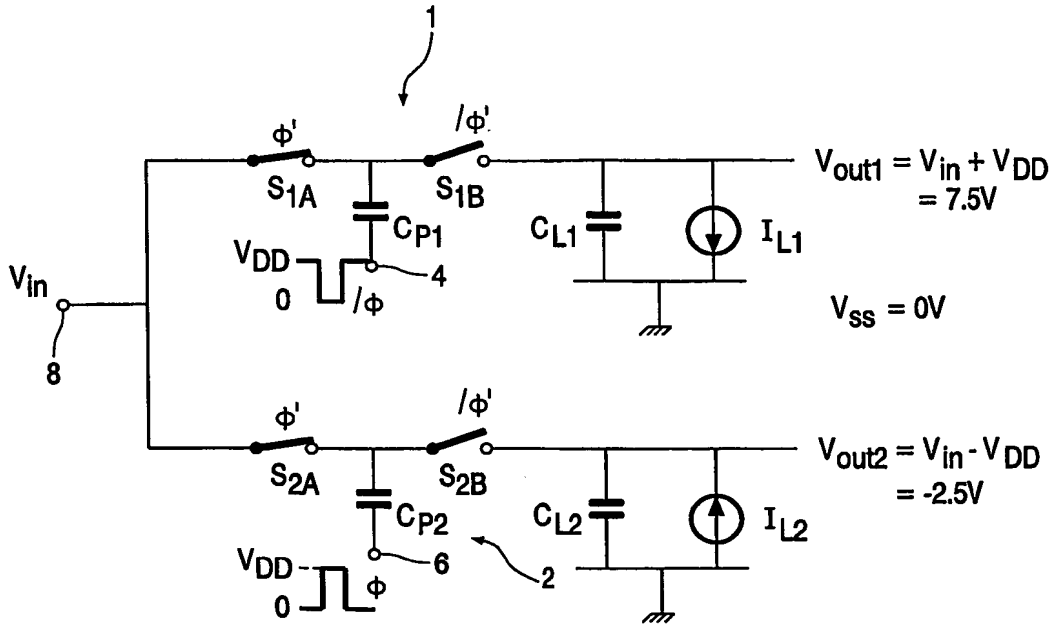
(84) Designated States *(regional)*: ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN,*

[Continued on next page]

(54) Title: A CHARGE PUMP CIRCUIT



(57) Abstract: A charge pump circuit has a voltage increasing stage and a voltage decreasing stage in parallel, and sharing a common input. This allows charge to flow between the stages, so that charge used in the pumping of one stage is recycled to the other stage.

WO 2004/066478 A1

IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DESCRIPTION

A CHARGE PUMP CIRCUIT

This invention relates to a charge pump circuit. In particular, it relates to a charge pump circuit which is capable of providing voltage outputs which are not integer multiples of the supply voltages. The invention also relates to electronic devices including such a circuit, particularly but not exclusively, large-area electronic (LAE) devices such as an active matrix liquid crystal display (AMLCD) or another type of active matrix display. A semiconductor device or semiconductor integrated circuit is another device form, in which the charge pump circuit may, for example, be integrated.

Charge pump circuits are known for providing a boosted DC voltage from a lower DC voltage supply. The boosted voltage may be more positive than the high level of the input supply voltage or, alternatively, more negative than the low level of the input supply voltage. Such circuits may comprise a series of voltage boosting stages which each include a switch connected to a capacitor, the switch controlling the flow of charge onto the capacitor. Such a circuit is disclosed for example in WO 02/061930. The switch of each stage is provided at the input of the stage, and the output of each stage is the junction between the switch and capacitor. The input to the circuit is a DC current supply at the lower voltage magnitude. The capacitors are connected alternately to one of two complementary clocked control lines which control the switching operation, which in turn controls the so-called pumping of charge along the series of stages.

During operation of the circuit, one clock cycle causes a charge stored on the capacitors connected to one of the control lines to be passed to the capacitors of the respective next stage. The voltage across the capacitors increases progressively along the series of voltage boosting stages. A larger number of stages leads to a larger output voltage for the circuit.

For a given power supply with a low voltage level of V_{SS} = 0V (for the sake of explanation only) and a high voltage level of V_{DD}, charge pump circuits

of the type disclosed in WO 02/061930 are used to generate a voltage of $(n+1)V_{DD}$ in the case of a positive charge pump and $-nV_{DD}$ in the case of a negative charge pump, where n is an integer equal to the number of stages in the charge pump. However, it is often the case that the output voltage required is not equal to an integer multiple of the power supply voltage V_{DD}. In this case, it is known to use additional circuitry to regulate the output voltage to the required value, which provides a fundamental limit to the theoretical efficiency that can be achieved.

For example, a single stage positive charge pump with a 5V input voltage would normally generate an output voltage of 10V. If this is regulated down to a required output voltage of 7.5V, the maximum theoretical efficiency of the charge pump is reduced to 75%.

US 5 790 393 discloses a charge pump circuit for generating a fractional multiple of the supply voltage. The capacitor storing the pumped charge is connected in parallel with an additional capacitor at the output of the circuit in order to reduce the output voltage to a level which is the required fractional multiple. Although this circuit does not use a voltage regulator, it also has the disadvantage of a limited maximum theoretical efficiency.

In addition to providing fractional multiples of the voltage supply lines, there is often a need both for a voltage above that of the high voltage supply line and a voltage below that of the low voltage supply line.

One example of an application of charge pump circuits is in portable electronic devices having display screens. A relatively high voltage is needed for the display, for example 15V, whereas the device is to be powered by a relatively low voltage supply, for example 3V. The use of a voltage boosting device such as a charge pump circuit is clearly appropriate.

According to the invention, there is provided a charge pump circuit comprising:

a voltage increasing stage;

a voltage decreasing stage in parallel with the voltage increasing stage; and

a shared input to the voltage increasing and voltage decreasing stages.

The invention addresses the problem of generating two (or possibly more) boosted voltages, one of which is in the positive sense and one of which is in the negative sense relative to the power supply voltages. Furthermore, the circuit enables voltages to be generated which are not equal to an integer multiple of the power supply voltage. In particular, charge used in the pumping of one stage can be recycled to the other stage, as the voltage increasing stage and the voltage decreasing stage require charge pumping in opposite senses. Thus, an efficient means of generating the required voltages is provided.

The voltage increasing stage is preferably for increasing an input voltage by an integer multiple of the difference between a low supply line voltage and a high supply line voltage and the voltage decreasing stage is for decreasing an input voltage by an integer multiple of the difference between a low supply line voltage and a high supply line voltage. By selecting the input voltage at a value between the supply line voltages, the output voltages are non-integer multiples of the supply line voltages.

The voltage increasing stage may comprise one or more charge pump sections, each for increasing the input voltage by the difference between a low supply line voltage and a high supply line voltage. Similarly, the voltage decreasing stage may comprise one or more charge pump sections, each for decreasing the input voltage by the difference between a low supply line voltage and a high supply line voltage.

Each charge pump section preferably comprises an input switch and an output switch in series connected together at a junction node, and a charge pump capacitor connected between junction node and a control line.

Each charge pump section may comprise a first input switch and output switch in series connected together at a first junction node, a second input switch and output switch in series connected together at a second junction node, a first charge pump capacitor connected between the first junction node and a first control line and a second charge pump capacitor connected between the second junction node and a second control line. This provides

two pump circuits in parallel, so that charge pumping can be performed during all clock cycles.

In another arrangement each charge pump section of the voltage increasing stage and of the voltage decreasing stage may comprise a first input switch and output switch in series connected together at a first junction node, and a second input switch connected between the input and a second junction node, a first charge pump capacitor connected between the first junction node and a first control line and a second capacitor connected between the second junction node and a second control line, wherein the second junction node provides the control signals for the first input and output switches.

In this arrangement, only one charge pump capacitor is provided in each charge pump circuit, and the other capacitor is for generating appropriate switch control signals. Complementary signals are again applied to the first and second control lines. However, in both arrangements, non-overlapping signals may be used instead.

The invention also provides an integrated circuit device or other electronic device which may be formed using, for example, low temperature poly-silicon processing and which includes a charge pump circuit of the invention. The device may comprise an active matrix liquid crystal display device, with the charge pump circuit and a TFT switching array for the display being provided on a common substrate.

Embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a schematic circuit diagram of a charge pump circuit in accordance with the invention;

Figure 2 is a more detailed circuit diagram showing one implementation of the circuit of Figure 1; and

Figures 3A and 3B are used to explain in greater detail the operation of the circuit of Figure 2; and

Figure 4 is a more detailed circuit diagram showing another implementation of the circuit of Figure 1;

Figure 5 is a schematic plan view of a LAE device incorporating a display and a charge pump circuit; and

Figures 6 to 11 illustrate schematically further, alternative, embodiments of charge pump circuits in accordance with the invention.

The same reference numbers and symbols are used throughout the Figures to denote the same or similar features.

The invention provides a circuit capable of generating two (or possibly more) boosted voltages, one of which is in the positive sense and one of which is in the negative sense relative to the power supply voltages. Furthermore, the circuit enables these voltages to be equal to non-integer multiples of the power supply voltage. This provides an efficient way of generating voltages for example for an analogue switch, where it may be necessary to generate voltages above and below the power rails in order to ensure the switch can be properly turned on and off. This capability is required in a large number of analogue circuit applications.

Figure 1 shows in schematic form a charge pump circuit in accordance with the invention, for illustrating the basic idea behind the invention.

The circuit includes a voltage boosting stage 1 and a voltage decreasing stage 2. Each stage has an input switching device S_{1A}, S_{2A} (referred to generally as S_{nA} in the following) and a charge pump capacitor C_{P1}, C_{P2} (referred to generally as C_{Pn} in the following) connected in series between the input to the stage and a respective voltage control terminal 4, 6. The output from each stage 1, 2 comprises the node between the switching device S_{nA} and the capacitor C_{Pn}. This node is connected to the output of the stage through an output switch S_{1B}, S_{2B} (referred to generally as S_{nB} in the following).

The input and output switches S_{nA}, S_{nB} are switched with complementary signals (Φ' and /Φ') so that the charge pump capacitor is alternately connected to the input 8 and to the output of the stage.

The voltages on the voltage control terminals 4, 6 are switchable between two levels. This is achieved by providing a square tooth waveform to the terminals 4,6. The voltages supplied to the control voltage terminals 4 and 6 alternate voltage levels corresponding to the voltages of a high voltage supply rail and a low voltage supply rail. For example, the low voltage supply rail may be a ground connection.

The voltage on one terminal 4 (/Φ) is the complement of the voltage on the other 6 (Φ), so that one signal has opposite polarity to the other, but is clocked at the same time.

The same control signal waveform timing may be used for the control of the input and output switches as for the control lines 4,6. In other words Φ can have the same transitions as Φ'. Thus, when CP1 is connected to the low voltage and CP2 is connected to the high voltage, switches S1A and S2A are closed (low impedance) and S1B and S2B are open (i.e. high impedance). Similarly when CP1 is connected to the high voltage and CP2 is connected to the low voltage, switches S1A and S2A are open (high impedance) and S1B and S2B are closed (low impedance). The actual nature of the control signals Φ' and /Φ' depends upon the nature of the switches.

In operation of each stage, a DC input voltage Vin is applied to the input 8 of the charge pump circuit. This voltage source supplies a mean current that is approximately equal to the difference in the mean load currents drawn at the outputs, so $I(Vin) = I_{L1} - I_{L2}$. If I_{L2} is greater than I_{L1}, the Vin will sink current, whereas if I_{L1} is greater than I_{L2} it will supply current.

Taking the voltage boosting stage 1 by way of example, when the input switch S_{1A} is closed, charge flows to the capacitor C_{P1}, to charge it to the input voltage (less any voltage drop across the switch). This charge is provided to the capacitor when the control terminal 4 is connected to the low control voltage (e.g. 0V) and the input switch is closed. At the next clock cycle, and after the capacitor has charged, the switch S_{1A} is opened, and the voltages on

the control terminals are reversed. The voltage across the capacitor C_{P1} will then add to the new higher voltage (e.g. 5V) on the control terminal 4, so that an increased voltage appears at the output of the stage.

This increased output voltage is provided to the output through the closed output switch S_{1B}.

The voltage decreasing stage 2 in Figure 1 operates in similar manner, but provides a step decrease in the voltage corresponding to the magnitude of the voltage difference between the high and low power rails (shown as 0V and V_{DD} in Figure 1).

The operation of the circuit is achieved after an initial settling period which is required for the output voltages to reach their steady state levels. The output voltages rise and fall around this steady state level as charge is pumped along the circuit and current is supplied to the load. The magnitude of this ripple is reduced by increasing the size of the capacitors connected at the output of the charge pumps. The charge pumping operation is well known and will not be described in further detail.

In accordance with the invention, the voltage boosting and voltage decreasing stages 1, 2 share a common input Vin. The input voltage Vin lies between the power supply rail voltages. In conventional circuits, a negative charge pump would have its input connected to the low voltage supply rail and the positive charge pump would have its input connected to the high voltage supply rail V_{DD}. By connecting together the two inputs, the efficient generation of non-integer multiples of the power supply voltage is provided, because charge injected by the voltage decreasing charge pump can be recycled back into the voltage increasing charge pump. This minimises the current that must be supplied by the voltage source Vin.

Decoupling capacitors C_{L1} and C_{L2} are provided at the outputs, and connected to ground. These capacitors could in fact be connected to any low impedance constant voltage source. The decoupling capacitors are charged (i.e. pumped) to the output voltage during the start-up phase. They serve to minimise the ripple in output voltage during operation (the larger they are the lower the ripple). This is required because the charge on C_{L1} and C_{L2} is

topped up once per clock cycle, but the load is likely to draw current continuously. The decoupling capacitors are likely to be off-glass external components.

The operation of the circuit will now described in further detail assuming the low power line voltage V_{SS} to be 0V and the high power line voltage to be V_{DD}. The circuit in Figure 1 generates a positive output voltage Vout1 = Vin + V_{DD} and a negative output voltage Vout2 = Vin – V_{DD}, where Vin is a voltage between 0 and V_{DD}.

Although the difference between Vout1 and Vout2 is always equal to $2V_{DD}$, the absolute levels of Vout1 and Vout2 can be adjusted from between $2V_{DD}$ and 0V respectively at the upper end down to V_{DD} and $-V_{DD}$ respectively at the lower end, depending on the value of Vin. This circuit offers advantages over conventional approaches when the required output voltages lie between these two limits. This is because the negative charge pump that generates Vout2 injects charge back towards the input voltage source Vin. However, at the same time the positive charge pump that generates Vout1 draws charge from the voltage source Vin. Consequently, the net effect is that charge from the negative charge pump can be recycled back into positive charge pump.

Figure 1 also represents the load driven by the two generated voltages as a first current source I_{L1} connected between the boosted voltage and the low power supply line voltage (ground in this example), and a second current source I_{L2} connected between the reduced voltage and the low power supply line voltage. These load currents depend upon the load driven by the circuit.

If the load currents I_{L1} and I_{L2} are equal, there is no net current flow into or from the voltage source Vin, which means that the voltage source can be designed with a high resistance. In the case where Vin is a voltage source with 100% efficiency, the charge pump switches are ideal and the pump capacitors are infinite, the theoretical efficiency is equal to 100% provided that I_{L1} is greater than or equal to I_{L2}. If I_{L1} is less than I_{L2} and charge injected into the voltage source Vin cannot be recycled, then the efficiency decreases accordingly.

The circuit in Figure 1 shows charge pumps formed using switches, but diodes could instead be used. Also, the positive and negative charge pumps illustrated in Figure 1 have only a single stage.

The principle can be easily extended to charge pumps with multiple stages, in which case the positive output voltage becomes $Voutp = Vin + nV_{DD}$ (where n is the number of stages in the positive charge pump) and the negative output voltage becomes $Voutn = Vin - mV_{DD}$ (where m is the number of stages in the negative charge pump).

In a multiple stage arrangement, charge flows (or is pumped) from the capacitor in one stage to the capacitor in the next. The capacitor in next stage has the opposite control voltage applied to it at this time, so that the capacitor of this next stage has a higher voltage across it than the voltage across the capacitor in the previous stage. The capacitor voltage thus increases along the series of stages.

The voltage across one capacitor will be greater than the voltage across the previous capacitor by the difference between the control voltages (ignoring the voltage drop across the switches). This is the so-called boost voltage.

In a chain of charge pumps, adjacent pumps are controlled by complementary control signals, so that there are two voltage control terminals each associated with a different set of voltage boosting stages.

There can also be a number of positive charge pumps (each with a number of stages) and a number of negative charge pumps (each with a number of stages) connected to the same input voltage source Vin. Again, the criteria for obtaining the optimum efficiency due to charge recycling is that the current injected by negative charge pumps back towards the input voltage source Vin should be less than or equal to the current drawn by the positive charge pumps from the source Vin.

In order to ensure that the current is properly recycled from the negative to the positive arms of the charge pumps, some care may be required in the design of the voltage source Vin. Specifically, it may be necessary to design it with a particular résistance and to use a decoupling capacitor on the output. This is a known technique. Also if the load current in the positive arms is less

in magnitude than the load current in the negative arms so that current is drawn from the voltage source Vin, it is desirable that Vin should be made as efficient as possible. Circuits for efficiently generating a voltage between the power supply voltages are also well known. For example a capacitive divider circuit can generate $V_{DD}/2$ with an ideal efficiency (assuming ideal switches an infinite capacitors) of 100%.

A more detailed example of a circuit implementation is shown in Figure 2, again each of the charge pumps consists of a single boosting stage, for simplicity. The output loads are represented as resistors R_{L1} and R_{L2} in Figure 2. In Figure 2, NMOS transistors are designated as "N" and PMOS transistors are designated as "P".

The voltage increasing stage 1 and the voltage decreasing stage 2 are implemented using poly-silicon TFTs (thin film transistors) and suitable for integration into an active matrix LCD display with input supply voltages of 5V and 0V. From these input voltages, the circuit is used to generate +7.5V and –2.5V, which are required for CMOS switches to ensure they can be properly turned on and off.

Each stage 1, 2 is associated with two charge pump capacitors C_{p1a}, C_{p1b} and C_{p2a}, C_{p2b}. Each capacitor connects to the junction between an input transistor switch N_{1a}, N_{1b}, P_{2a}, P_{2b} and an output transistor switch P_{1b}, P_{1a}, N_{2a}, N_{2b}. Thus, each stage effectively comprises two of the charge pump arrangements shown in Figure 1, arranged in parallel with each other. This arrangement enables charge pumping to be performed during all cycles.

In Figure 2, the two charge pumps in parallel enable appropriate gate voltages to be generated simply for the input and output switches, which are implemented as transistors. These gate voltages have a transition of equal magnitude to the clock transition, but both levels are shifted up (or down) by an amount equal to Vin.

The switches may instead be implemented as diodes, and no control signal are then required, as the diodes turn on and off as a natural consequence of the way the charge pump circuit functions.

The operation of each stage will be described in detail with reference to Figures 3A and 3B.

Figure 3A shows the components of the voltage boosting stage 1. Voltages are indicated in the Figure assuming the low power rail to be 0V and the high power rail to be 5V. Figure 3A shows the cycle in which the upper control terminal is at the low voltage and the lower control terminal is at the high voltage. The transistors and capacitors have not been given references in Figure 3A and 3B, as they correspond to those of Figure 2. The references of Figure 2 are thus used to identify the corresponding components in Figure 3. The arrows in Figures 3A and 3B represent the flow of charge.

The input voltage of 2.5V charges the upper capacitor C_{p1b} to 2.5V through transistor N_{1b} which is turned on. The equilibrium at the output is 7.5V, and as shown the lower capacitor C_{p1a} is charged with 2.5V across it and thereby presents 7.5V to the output. Charge is pumped to the output through transistor P_{1a} to maintain the output at this voltage.

Figure 3B shows the cycle in which the upper control terminal is at the high voltage and the lower control terminal is at the low voltage.

The input voltage of 2.5V charges the lower capacitor C_{p1a} to 2.5V through transistor P_{1a} which is turned on. The upper capacitor C_{p1b} is charged with 2.5V across it and presents 7.5V to the output. Charge is pumped to the output through transistor P_{1b} to maintain the output at this voltage.

This arrangement thus provides charge pumping during all clock cycles.

The voltage decreasing stage 2 operates in the same way, although with charge flowing in the opposite direction.

As shown in Figure 2, the charge pump section of the voltage increasing stage 1 the charge pump section of the voltage decreasing stage 2 are connected together by the charge pump capacitors C_{p1a} and C_{p2a} which are connected together in series, with one of the control lines at the junction.

The circuit of Figure 2 has two charge pump capacitors for each charge pump stage. These capacitors need to be of a certain size to perform the charge pump operation, and this increases the area needed by the circuit.

Figure 4 shows an alternative implementation with just one pump capacitor per charge pump stage, Cp1 and Cp2. Each charge pump stage also has only one output switch P1 and N2. Accordingly, charge pumping is performed by each stage during only one of the two cycles.

In the voltage increasing stage, one input switch N1b and capacitor Cbs1 are only used to generate a level shifted clock to drive the gate signals for the other input switch N1a and the output switch P1. Similarly, in the voltage decreasing stage, the input switch P2b and the capacitor Cbs2 are only used to generate a level shifted clock for the gates of the input switch P2a and the output switch N2.

As capacitors Cbs1 and Cbs2 are not used to pump charge into the circuit, their value can be much smaller than Cp1 and Cp2. This circuit is preferred, particularly if the values of Cp1 and Cp2 are too big to enable them to be integrated onto the glass.

Figure 5 shows an integrated circuit device 30 including an active matrix liquid crystal display device which uses a TFT switching array 32. The switching array and a charge pump circuit 34 are provided on a common substrate 36, and a low voltage power supply 38 (for example a 3V battery) provides power to the integrated circuit 36.

Figure 6 shows the same basic charge pump circuit as in Figure 1, but with the timing of the control signals applied to switches S1A, S1B, S2A, S2B and control terminals 4 and 6 modified. In this case the timing of the control signals applied to S1B and S2A is the same as the timing of the waveform applied to terminals 4 and 6. This means that when terminals 4 and 6 are connected to the high voltage level VDD, switches S1B and S2A are closed (i.e. low impedance) and switches S1A and S2B are open (i.e. high impedance). Conversely, when terminals 4 and 6 are connected to the low voltage level, 0 Volts in Figure 6, switches S1B and S2A are open (i.e. high impedance) and switches S1A and S2B are closed (i.e. low impedance). This modification to the timing means there is a delay of half a clock period after charge is injected from the voltage decreasing stage 2 before it is recycled into the voltage increasing stage 1. In order to ensure that charge is properly

recycled it is necessary to decouple the voltage source Vin as mentioned earlier, and here this is achieved through a resistor Rin and capacitor Cin. In effect, the capacitor Cin acts as a temporary storage node for charge injected from the voltage decreasing stage 2 before it is recycled into the voltage increasing stage 1.

Figure 7 shows a possible circuit for implementing the schematic configuration shown in Figure 6. The circuit is the same as in Figure 4, but the clock signals applied to Cp1, Cp2, Cbs1 and Cbs2 have been modified so that the timing is as shown in Figure 6. Figure 7 also shows explicitly the resistor Rin and capacitor Cin used to decouple the voltage source Vin.

In the embodiments described so far the control signals applied to the switches in the charge pump and the voltages levels applied to the charge pump capacitors are complementary, which means all transitions take place simultaneously so that when a particular signal switches from low to high, its complement switches from high to low. It is known that the efficiency of charge pumps can be improved in some cases by using control signals that do not switch simultaneously. This will be referred to as the use of non-overlapping control signals. Non-overlapping control signals can be used to ensure that charge does not leak through the charge pump switches in the wrong direction during the finite time that they take to switch. The remaining examples show how non-overlapping control signals can be used in conjunction with this invention.

Figure 8 shows a schematic form of a charge pump with non-overlapping control signals ϕa and ϕb applied the charge pump switches and complementary waveforms ϕ and $/\phi$ applied to terminals 6 and 4. When ϕ switches to a high level terminal 6 is connected to the high power supply voltage and terminal 4 is connected to the low power supply voltage. During this transition all the switches S1A, S1B, S2A and S2B are open (i.e. high impedance). After a delay period a transition in ϕa causes S1A and S2A to close, which connects capacitors CP1 and CP2 to Vin. After a charging period, a further transition in ϕa causes S1A and S2A to open. After a delay period ϕ switches to a low level so terminal 6 is connected to the low voltage supply

and terminal 4 is connected to the high voltage supply. Then, after a further delay period a transition on ϕb causes S1B and S2B to close, which connects CP1 to CL1 and CP2 to CL2. Then after a further charging period a transition in ϕb causes S1B and S2B to open. This cycle is repeated continuously so that CL1 and CL2 are pumped to their respective output voltages as indicated in Figure 8.

Figure 9 shows a possible circuit for implementing the schematic configuration shown in Figure 8. Transistor N1b and capacitor Cbs1a in conjunction with control signal ϕa generate level shifted voltage signals for switching the charge pump transistor N1a. Transistor N1c and capacitor Cbs1b in conjunction with control signal $/\phi b$ generate voltage signals for switching the charge pump transistor P1. Transistor P2b and capacitor Cbs2a in conjunction with control signal $/\phi a$ generate voltage signals for switching the charge pump transistor P2a. Transistor P2c and capacitor Cbs2b in conjunction with control signal ϕb generate voltage signals for switching the charge pump transistor N2. This circuit requires the generation of 6 control signal ϕ, ϕa, ϕb and their complements.

Figure 10 shows a schematic form of a charge pump with non-overlapping control signals ϕa and ϕb applied the charge pump switches and a waveform ϕ applied to terminals 6 and 4. When ϕ switches to a low level terminals 4 and 6 are connected to the low power supply voltage. During this transition all the switches S1A, S1B, S2A and S2B are open. After a delay period a transition in ϕa causes S1A and S2B to close. This connects CP1 to Vin and CP2 to CL2. After a charging period, a further transition in ϕa causes S1A and S2B to open. After a delay period ϕ switches to a high level so terminals 4 and 6 are connected to the high voltage supply. Then, after a further delay period a transition on ϕb causes S1B and S2A to close, which connects CP1 to CL1 and CP2 to Vin. Then after a further charging period a transition in ϕb causes S1B and S2A to open. This cycle is repeated continuously so that CL1 and CL2 are pumped to their respective output voltages as indicated in Figure 8.

Figure 11 shows a possible circuit for implementing the schematic configuration shown in Figure 10. The basic circuit is the same as in Figure 9, but the control signals have been modified so that the switching sequence of the circuit is as shown in Figure 10. The advantage of this circuit is that it requires the generation of just three control signals ϕ, ϕa and ϕb compared with six control signals for the circuit in Figure 9. As described in the description of Figure 6 the decoupling of Vin, provided by Rin and Cin in Figures 10 and 11, is required to ensure charge is properly recycled from the voltage decreasing charge pump to the voltage increasing charge pump.

As previously mentioned, the charge pump circuit of the present invention may be used in large area electronic devices such as active matrix display devices and similar.

However, the charge pump circuit may be used with other types of device. Indeed, charge pumps are a very widely used circuit element found in many other applications. Examples include the generation of the programming and erase voltages for flash memories and in low voltage ICs where boosted voltages may be required by the analogue switches. Charge pumps may also be used in integrated control circuitry of a semiconductor power switch. The power switch may be, for example, a MOSFET. There are of course many more applications and various other modifications will be apparent to those skilled in the art.

CLAIMS

1. A charge pump circuit comprising:

a voltage increasing stage (1);

a voltage decreasing stage (2) in parallel with the voltage increasing stage; and

a shared input (8) to the voltage increasing and voltage decreasing stages.

2. A circuit as claimed in claim 1, wherein the voltage increasing stage (1) is for increasing an input voltage by an integer multiple of the difference between a low supply line voltage (V_{ss}) and a high supply line voltage (V_{DD}) and the voltage decreasing stage is for decreasing an input voltage by an integer multiple of the difference between a low supply line voltage (V_{SS}) and a high supply line voltage (V_{DD}).

3. A circuit as claimed in claim 1 or 2, wherein the voltage increasing stage comprises at least one charge pump section.

4. A circuit as claimed in claim 3, wherein the voltage increasing stage (1) comprises a plurality of charge pump sections, each for increasing the input voltage by the difference between a low supply line voltage and a high supply line voltage.

5. A circuit as claimed in any one of claims 1 to 3, wherein the voltage decreasing stage (2) comprises at least one charge pump section.

6. A circuit as claimed in claim 5, wherein the voltage decreasing stage comprises a plurality of charge pump sections, each for decreasing the input voltage by the difference between a low supply line voltage and a high supply line voltage.

7. A circuit as claimed in any one of claims 3 to 6, wherein the or each charge pump section of the voltage increasing stage (1) and of the voltage decreasing stage (2) comprises an input switch (S_{1A}; S_{2A}) and an output switch (S_{1B}; S_{2B}) in series connected together at a junction node, and a charge pump capacitor (C_{P1}; C_{P2}) connected between junction node and a control line (4;6).

8. A circuit as claimed in claim 7, wherein the or each charge pump section of the voltage increasing stage (1) and of the voltage decreasing stage (2) comprises a first input switch and output switch in series (N1a, P1a; P2a, N2a) connected together at a first junction node, a second input switch and output switch in series (N1b, P1b; P2b, N2b) connected together at a second junction node, a first charge pump capacitor (Cp1a;Cp2a) connected between the first junction node and a first control line (Φ) and a second charge pump capacitor (Cp1b;Cp2b) connected between the second junction node and a second control line (/Φ).

9. A circuit as claimed in claim 8, wherein complementary signals are applied to the first (Φ) and second (/Φ) control lines.

10. A circuit as claimed in Claim 8, wherein non-overlapping signals are applied to the first (Φ) and second (/Φ) control lines.

11. A circuit as claimed in claim 7, wherein the or each charge pump section of the voltage increasing stage (1) and of the voltage decreasing stage (2) comprises a first input switch and output switch in series (N1a,P1; P2a, N2) connected together at a first junction node, and a second input switch (N1b;P2b) connected between the input and a second junction node, a first charge pump capacitor (Cp1;Cp2) connected between the first junction node and a first control line and a second capacitor (Cbs1;Cbs2) connected between the second junction node and a second control line, wherein the

second junction node provides the control signals for the first input and output switches.

12. A circuit as claimed in claim 11, wherein complementary signals are applied to the first and second control lines.

13. A circuit as claimed in claim 11, wherein non-overlapping signals are applied to the first and second control lines.

14. A circuit as claimed in any one of claims 8 to 12, wherein the first input switch and output switch (N1a,P1; P2a,N2) are operated in complementary manner.

15. A circuit as claimed in any one of claims 8 to 14, wherein the charge pump capacitor of at least one charge pump section of the voltage increasing stage and the capacitor of at least one charge pump section of the voltage decreasing stage are connected together.

16. A circuit as claimed in any preceding claim, wherein the voltage increasing stage (1) is for increasing an input voltage by an integer multiple of the difference between a low supply line voltage and a high supply line voltage, the voltage decreasing stage (2) is for decreasing an input voltage by an integer multiple of the difference between a low supply line voltage and a high supply line voltage and wherein a voltage (Vin) is applied to the shared input (8) between the low supply line voltage and the high supply line voltage.

17. An electronic device (30) including a circuit (34) as claimed in any one of the preceding claims.

18. A device as claimed in claim 17, wherein the device (30) comprises a liquid crystal display.

19. A device as claimed in claim 18, wherein the circuit (34) and a TFT switching array (32) for the display are provided on a common substrate (36).

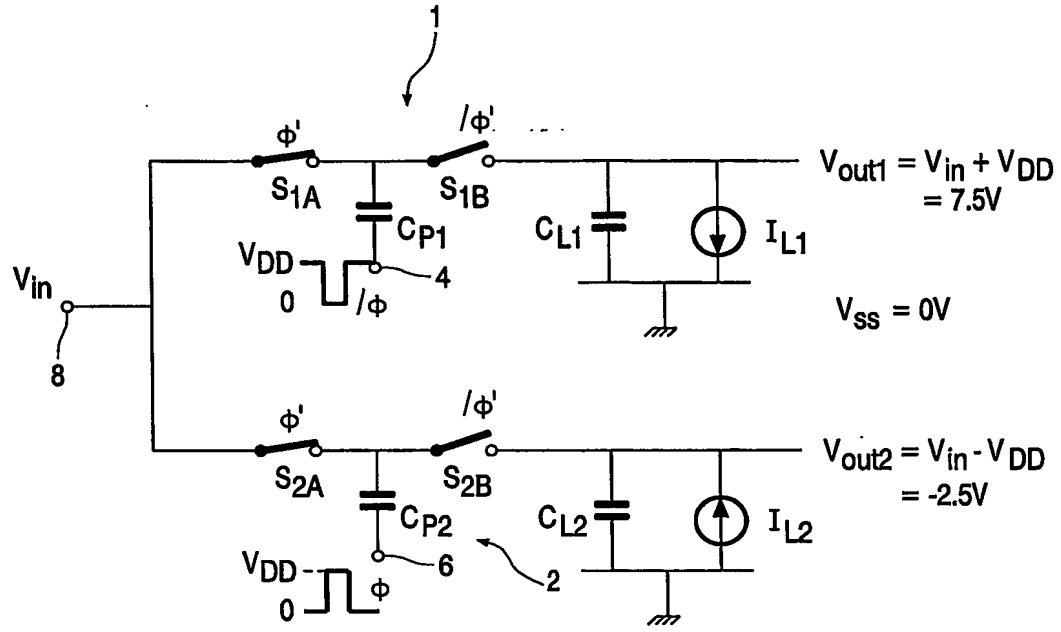

1
Φ'
/Φ'
S1A
S1B
CP1
CL1
IL1
VDD
0
/Φ
4
Vin
8
Vout1 = Vin + VDD
= 7.5V
Vss = 0V
Φ'
/Φ'
S2A
S2B
CP2
CL2
IL2
VDD
0
Φ
6
2
Vout2 = Vin - VDD
= -2.5V

FIG.1

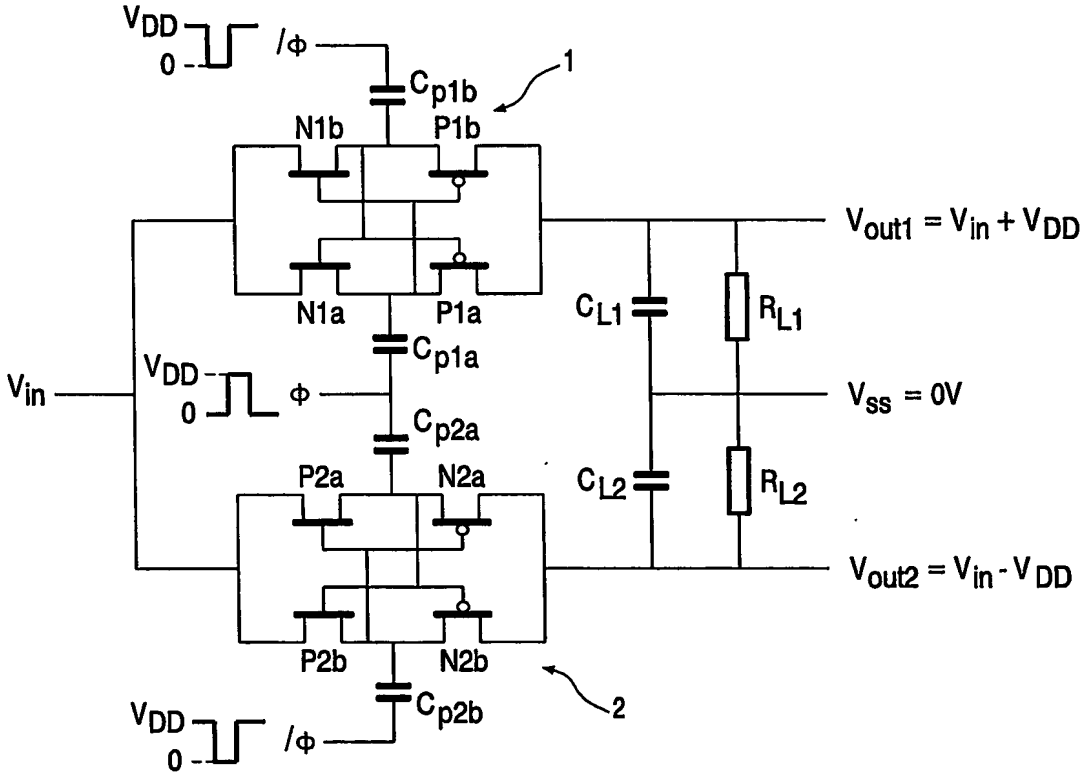

VDD
0
/Φ
Cp1b
1
N1b
P1b
N1a
P1a
Cp1a
Vin
VDD
0
Φ
Cp2a
P2a
N2a
P2b
N2b
Cp2b
VDD
0
/Φ
2
CL1
RL1
CL2
RL2
Vout1 = Vin + VDD
Vss = 0V
Vout2 = Vin - VDD

FIG.2

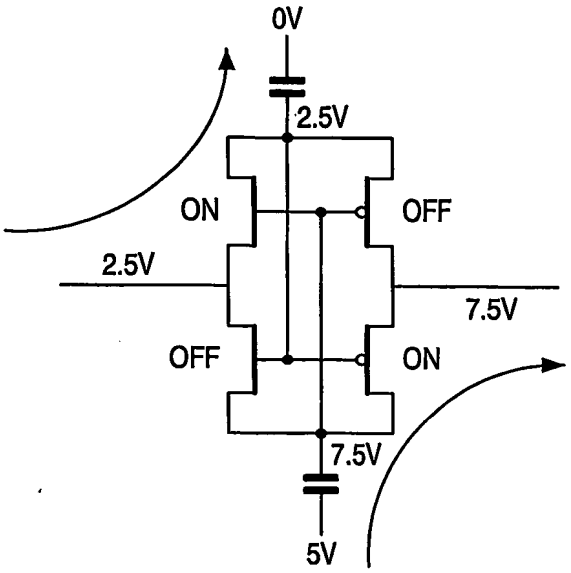

0V
2.5V
ON
OFF
2.5V
7.5V
OFF
ON
7.5V
5V

FIG.3A

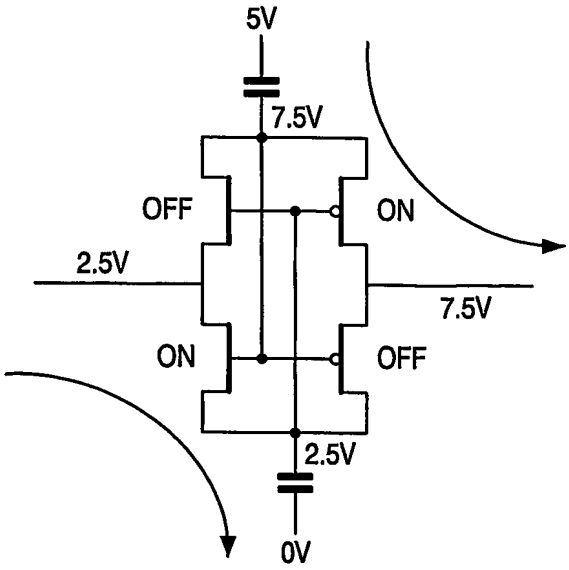

5V
7.5V
OFF
ON
2.5V
7.5V
ON
OFF
2.5V
0V

FIG.3B

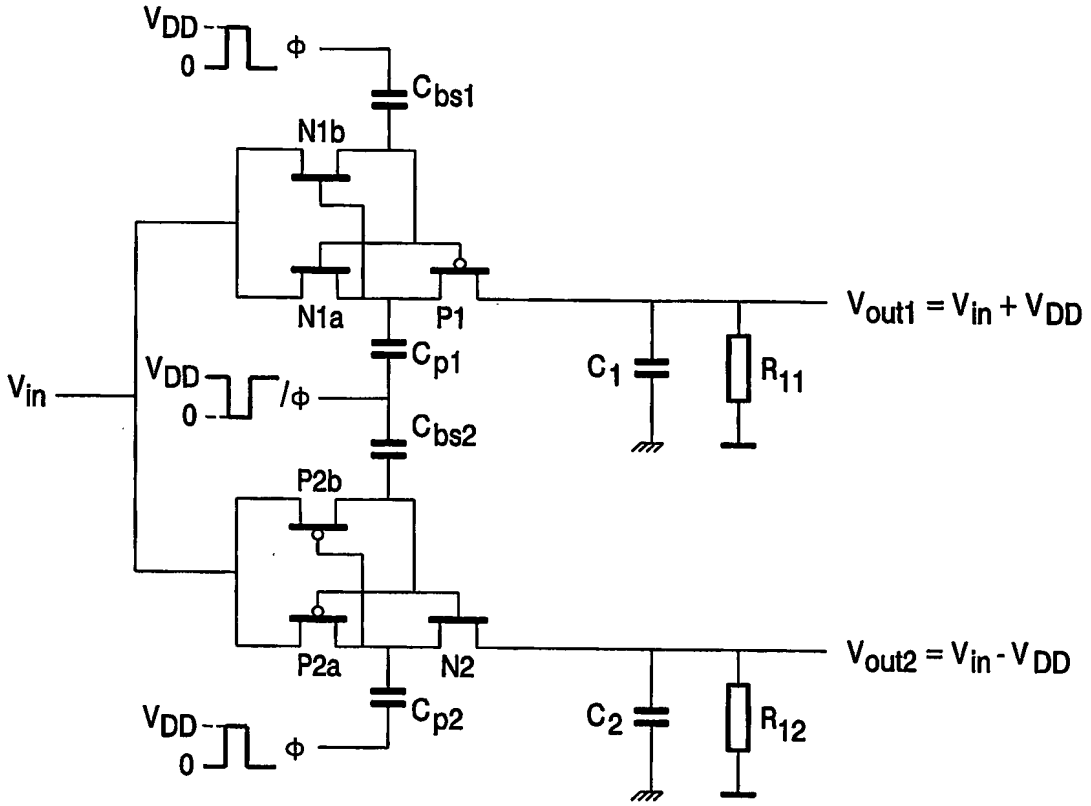

VDD
0
Φ
Cbs1
N1b
N1a
P1
Vout1 = Vin + VDD
Vin
VDD
0
/Φ
Cp1
C1
R11
Cbs2
P2b
P2a
N2
Vout2 = Vin - VDD
VDD
0
Φ
Cp2
C2
R12

FIG.4

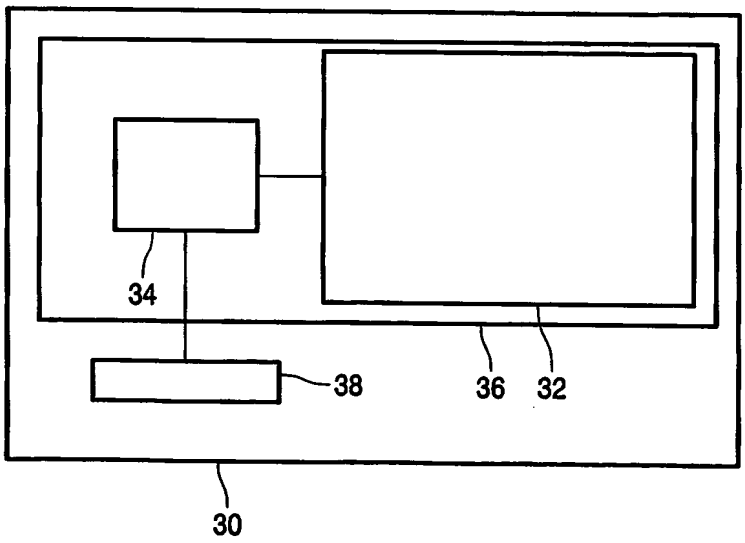

34
38
36
32
30

FIG.5

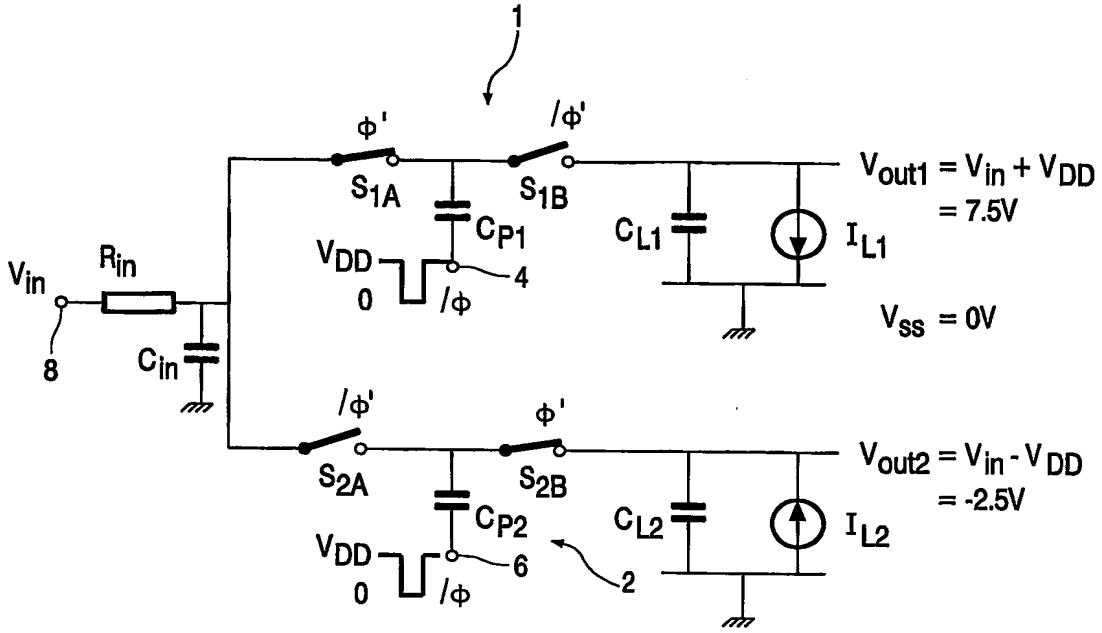

1
Φ'
/Φ'
S1A
S1B
CP1
VDD
0
/Φ
4
Vin
Rin
8
Cin
CL1
IL1
Vout1 = Vin + VDD
= 7.5V
Vss = 0V
/Φ'
Φ'
S2A
S2B
CP2
VDD
0
/Φ
6
2
CL2
IL2
Vout2 = Vin - VDD
= -2.5V

FIG.6

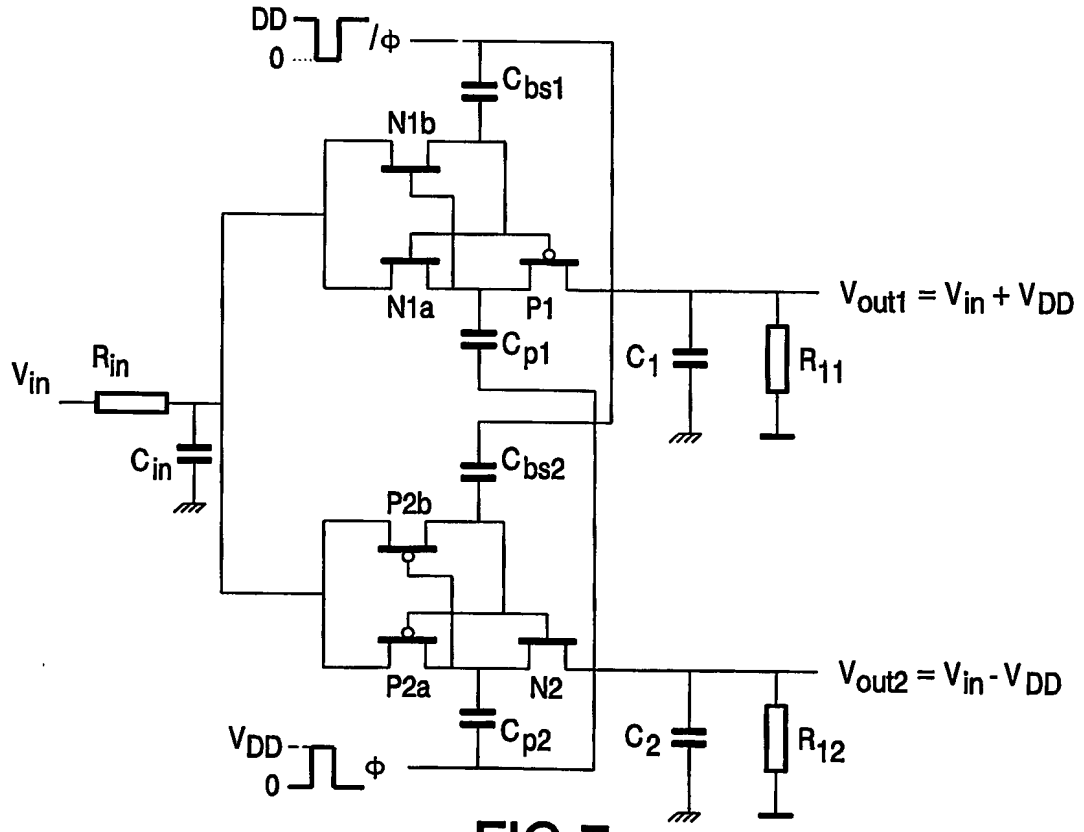

DD
0
/Φ
Cbs1
N1b
N1a
P1
Cp1
Vout1 = Vin + VDD
C1
R11
Vin
Rin
Cin
Cbs2
P2b
P2a
N2
Cp2
VDD
0
Φ
C2
R12
Vout2 = Vin - VDD

FIG.7

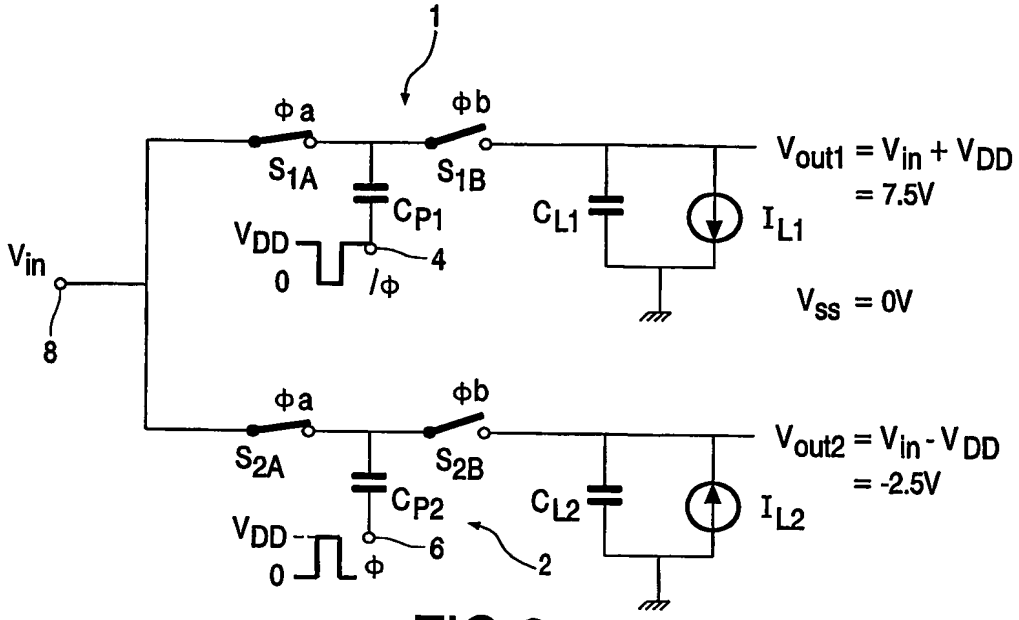

1
Φa
Φb
S1A
S1B
CP1
VDD
0
/Φ
4
Vin
8
CL1
IL1
Vout1 = Vin + VDD
= 7.5V
Vss = 0V
Φa
Φb
S2A
S2B
CP2
VDD
0
Φ
6
2
CL2
IL2
Vout2 = Vin - VDD
= -2.5V

FIG.8

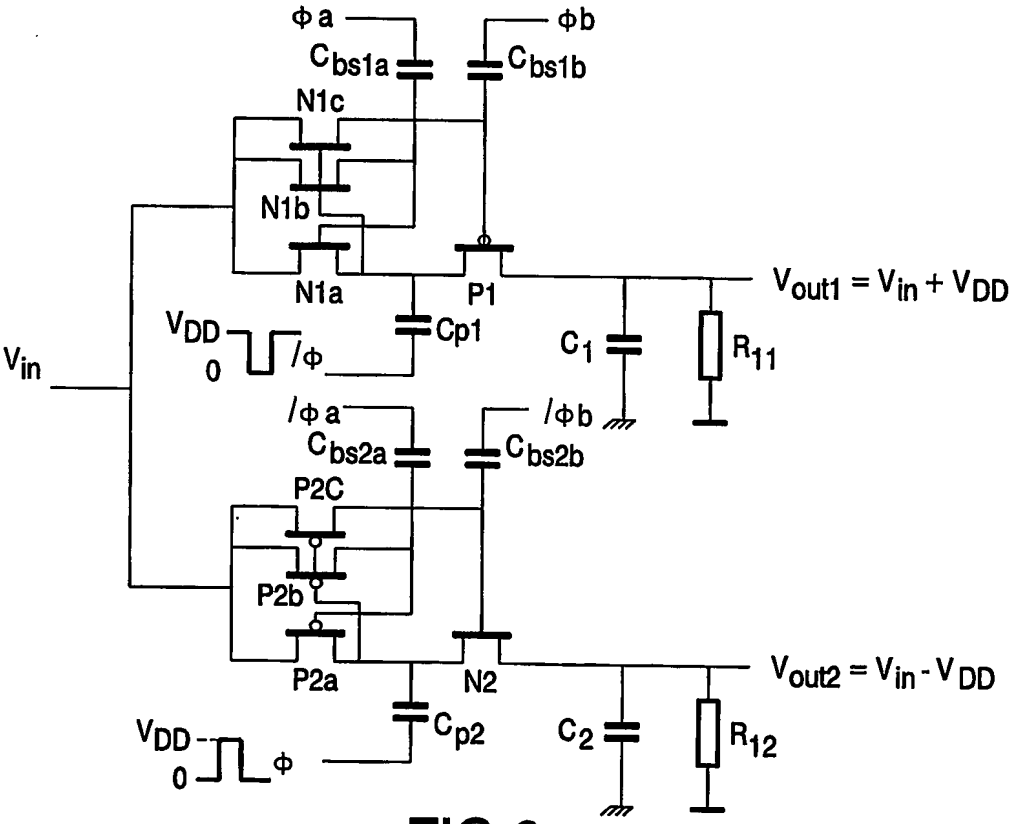

Φa
Φb
Cbs1a
Cbs1b
N1c
N1b
N1a
P1
Vout1 = Vin + VDD
VDD
0
/Φ
Cp1
C1
R11
Vin
/Φa
/Φb
Cbs2a
Cbs2b
P2C
P2b
P2a
N2
Vout2 = Vin - VDD
VDD
0
Φ
Cp2
C2
R12

FIG.9

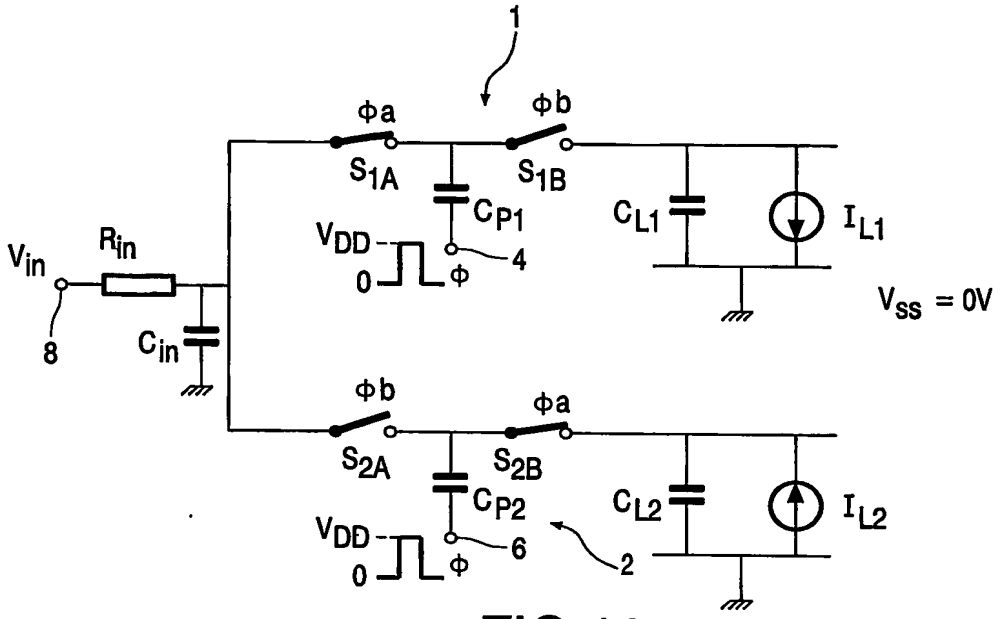

1
Φa
Φb
S1A
S1B
CP1
CL1
IL1
VDD
0
Φ
4
Vin
Rin
8
Cin
Vss = 0V
Φb
Φa
S2A
S2B
CP2
CL2
IL2
VDD
0
Φ
6
2

FIG.10

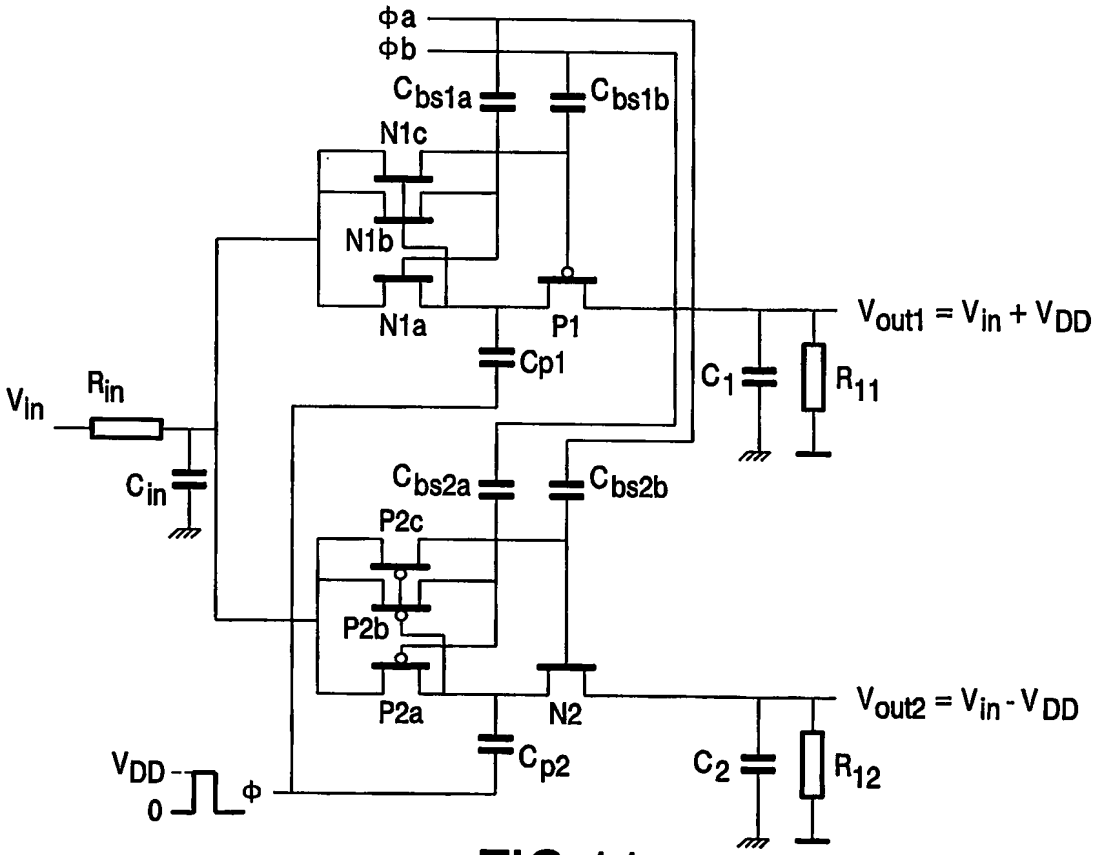

Φa
Φb
Cbs1a
Cbs1b
N1c
N1b
N1a
P1
Vout1 = Vin + VDD
Cp1
C1
R11
Vin
Rin
Cin
Cbs2a
Cbs2b
P2c
P2b
P2a
N2
Vout2 = Vin - VDD
Cp2
C2
R12
VDD
0
Φ

FIG.11

INTERNATIONAL SEARCH REPORT

Internation[illegible]ation No
PCT/IB 05/06352

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02M3/07

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2002/089369 A1 (IKEDA MASUHIDE) 11 July 2002 (2002-07-11) the whole document	1-3,5,7, 17,18 4,6, 8-16,19
X A	US 5 831 844 A (SUDO NAOAKI) 3 November 1998 (1998-11-03) the whole document	1,3-6,17 2,7,16, 18,19
X A	US 6 429 724 B1 (MIHARA MASAAKI ET AL) 6 August 2002 (2002-08-06) abstract; figures 1-3 column 4, line 55 -column 6, line 33 column 9, line 26 -column 10, line 57	1-3,5 4,6,7

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 March 2004	25/03/2004
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Thisse, S

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Internati[illegible]ion No
PCT/IB 0[illegible]6352

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 017, no. 440 (E-1414), 13 August 1993 (1993-08-13) & JP 05 091726 A (NEW JAPAN RADIO CO LTD), 9 April 1993 (1993-04-09) abstract	1
A	US 6 094 095 A (MURRAY KENELM ET AL) 25 July 2000 (2000-07-25) abstract; figure 1 column 1, line 30 -column 3, line 15	1

INTERNATIONAL SEARCH REPORT

Information [redacted] patent family members

Internatio [redacted] cation No
PCT/IB 03/06352

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 2002089369	A1	11-07-2002	JP	2002209375 A	26-07-2002
US 5831844	A	03-11-1998	JP	2845206 B2	13-01-1999
			JP	10066330 A	06-03-1998
US 6429724	B1	06-08-2002	JP	2000049299 A	18-02-2000
			TW	393644 B	11-06-2000
			US	6147547 A	14-11-2000
JP 05091726	A	09-04-1993	JP	3064573 B2	12-07-2000
US 6094095	A	25-07-2000	NONE		